



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/540,268

06/23/2005

Mitsuo Usami

843.45150X00

1433

20457

7590

08/05/2008

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER

SYED, NABIL H

ART UNIT

PAPER NUMBER

2612

MAIL DATE

DELIVERY MODE

08/05/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/540,268	Applicant(s) USAMI, MITSUO	
	Examiner NABIL H. SYED	Art Unit 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 May 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 6-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The following is a non-final office action in response to the RCE filed 5/23/08.

Amendments received on 5/23/08 have been entered. Claims 7-24 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 7 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 7 and 14 recite the limitation, "a memory address counter in which its count value indicates a bit address of **the memory pertaining to the first information.**" Specification discloses that "the memory address counter 13 is a counter indicating bit address of the memory 16 and has the same bit number as the first random number 11." Memory 16 has first information 17 and second information 11. It is unclear to the examiner that memory address counter is indicating the bit address of the first information or the second information. Further, from the claim language, the function of the memory address counter in the invention is unclear to the Examiner. More information is required regarding the memory address counter.

4. Claim 7 recites the limitation "the counter" in line 7. There is insufficient antecedent basis for this limitation in the claim. "The counter" should be -- the memory address counter--.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7-9, 14, 15, 19-21, 22-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bandy et al. (6,002,344) in view of Heng (6,538,563).

As of claim 7, Bandy discloses an IC tag (via a RFID tag 102, see fig. 3) for transmitting first information to a reception unit, comprising:
a memory which memorizes the first information (via tag having the tag ID as the first information) and second information (via tag 102 having a manufacture number; see col. 3, lines 8-17) (note: it is inherent that RFID tag have memory to store the identification number and other data to transmit to the reader) (see col. 3, lines 8-18);
and a memory address counter in which its count value indicates a bit address of the first memory (via counter/shift register 312, see fig 3) (also see col. 5, lines 4-8) (note: Bandy discloses that the tag transmits it tag ID when the value in the counter is same as

of tag ID, since the ID is stored in the memory and the counter is indicating the value of the ID, Bandy discloses a counter in which its value indicates a bit address of the memory; see col. 5, lines 4-9) (In the office action, below the tag ID, manufacture number and the lot number can be used as first information and second information and third information since claims does not specify which information is indicating the tag ID number or other numbers)

wherein the IC tag carries out count-up or count-down of a count value of the counter according to a clock signal received from the reception unit (via counter 312 increment its count when it receives the clock signal from the reader unit; see col. 1, lines 63-67) and the IC tag sets the second information of the second memory as an initial value of the counter and after the count value of the counter reaches a specified code, the first information stored in the bit address indicated by the count value is sent out to the reception unit successively (via tag transmitting the tag ID or manufacture number or lot number when the counter value matches any one of the tag ID or manufacture number or lot number (see col. 7, lines 12-33; also see col. 5, lines 4-20).

However Bandy fails to explicitly disclose that the second information control the time of transmission of the first information to the reception unit.

Heng discloses an IC tag (via transponder 1) which comprises a first information (via ID code 16; see fig. 8) and second information (via random number generator 12, generating a random number; see fig. 8, also see col. 4, lines 7-16). Heng discloses that the second information (random number) controls the time of transmission of the ID code to the interrogator 2 (via transponder 1 transmitting the ID code to the interrogator

at the time when the counter value is equal the random number generated by the random number generator; see col. 4, lines 17-28).

From the teaching of Heng it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Bandy to include use the second information to control the time of transmission of the first information to the reception unit as taught by Heng in order to avoid collision and expedite the process of interrogation.

As of claim 8, Bandy discloses that the memory memorizes the third information (via tag 102 memorizing a lot number; see fig. 3) and the IC tag sets either the second information or the third information as an initial value of the counter (note: Bandy discloses that if the third tag identifier does not resolve the contention, further reading can be done by adding more identification numbers in the tag (see col. 4, lines 7-12).

As of claim 9, Bandy discloses that the IC tag selects the second information or the third information by means of the mode switching portion and sets it as an initial value of the counter (via instruction interpreter 312 indicating which of the three numbers (tag ID, manufacture, lot number) are requested by the reader by telling the tag which of the read cycle is being performed) (see col. 5, lines 22-27).

As of claim 14, Bandy discloses a reading method for reading the first information from an IC tag having a memory (note: it is inherent that RFID tag have a memory to store the identification number and other data) which memorizes first information and second information (via Bandy discloses that a tag 102 have more than two information numbers, a tag ID number, a manufacture number and a lot number; see col. 3, lines 8-

18; see fig. 3), and a memory address counter (via a counter/shift register 312, see fig 3) in which a count value thereof indicates a bit address of the first memory to the reception unit (via conter/shiftregister transmitting the response signal to the reader unit, during first read cycle, which is equal to the tag ID; see col. 7, lines 1-30), comprising:

transmitting a clock signal from the reception unit to the IC tag (via tag reader 104(see fig. 1,) transmitting a clock signal; see col. 1, lines 63-67).

setting the second information stored in the memory as an initial value of the memory address counter as an initial value of the counter (note: Bandy discloses that during the first read cycle clock increment instruction from the reader unit makes the tag to increment the counter 312 until the output matches the tag ID, see col. 6, lines 64-67 through col. 7, lines 1-11) ;

performing count-up or count-down of a count value of the counter according to the clock signal (see col. 1, lines 63-67); and

after the count value of the memory address counter reaches a specified code, transmitting the first information stored in the bit address of the first memory indicated with the count value successively to the reception unit (via tag transmitting the tag ID or manufacture number or lot number when the counter value matches any one of the tag ID or manufacture number or lot number (see col. 7, lines 12-33; also see col. 5, lines 4-20).

However Bandy fails to explicitly disclose that the second information control the time of transmission of the first information to the reception unit.

Heng discloses an IC tag (via transponder 1) which comprises a first information (via ID code 16; see fig. 8) and second information (via random number generator 12, generating a random number; see fig. 8, also see col. 4, lines 7-16). Heng discloses that the second information (random number) controls the time of transmission of the ID code to the interrogator 2 (via transponder 1 transmitting the ID code to the interrogator at the time when the counter value is equal the random number generated by the random number generator; see col. 4, lines 17-28).

From the teaching of Heng it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Bandy to include use the second information to control the time of transmission of the first information to the reception unit as taught by Heng in order to avoid collision and expedite the process of interrogation.

As of claim 15, Bandy discloses that memory memorizes the third information and the second information is selected according to the mode switching signal and set up in the IC tag as an initial value of the counter (via sending the first read, second read and third read instruction to read tag ID, manufacture number and lot number respectively see col. 13, lines 14-24).

As of claim 19-21, Bandy discloses the IC tag wherein the counter and the second memory have the same bit number (via counter/shiftregister 312 and Tag ID having the same value, see col. 5, lines 5-9).

As of claim 22-24, Bandy discloses the IC tag wherein the first information is comprised of at least identification number and an error detection code for detecting an

error in the identification number (note: Bandy discloses this function by tag having a tag ID and a error code in case the contention occurs. For example tag can transmit its error-code using checksum (see col. 3, lines 48-55) and wherein the second information is a random number (via storing the tag ID's or manufacture number and lot number at the time of manufacturing; see col. 3, lines 1-17) .

As of claim 25 and 26, Heng discloses that the second information is a random number (via random number generating a random number; see col. 4, lines 20-25).

As of claims 27-30, Heng discloses that the first information identifies the IC tag (via IC code 16 identifying the transponder; see col. 4, lines 15-16).

7. Claims 10, 12, 13, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bandy et al. (6,002,344) and in view of Raimbault et al. (6,177,858).

As of claim 10, Bandy discloses all the elements of the claimed invention as mentioned in claim 9 above abut fails to explicitly disclose that the mode switching portion is a flip-flop.

Raimbault discloses an IC tag (via an electronic tag, fig. 1) wherein the mode-switching portion is a flip-flop (via electronic tag having a flip-flop in the logic circuit 4 to change the state of the tag; see fig.1, also see col. 7, lines 64-67 and col. 8, lines 1-7).

From the teaching of Raimbault it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the tag of Bandy to include a flip-flop in order to make the transponder easily switch between the read mode and transmit mode (see col. 11 and 18).

As of claim 12, Bandy discloses the IC tag wherein the counter and the second information have the same bit number (via counter/shiftregister 312 and Tag ID having the same value, see col. 5, lines 5-9).

As of claim 13, Bandy discloses the IC tag wherein the first information is comprised of at least identification number and an error detection code for detecting an error in the identification number (note: Bandy discloses this function by tag transmitting its ID and error code. For example tag can transmit its error-code using checksum (see col. 3, lines 48-55)).

8. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bandy et al (6,002,344) and in view of Chan (5,550,547).

As of claims 16-17 Bandy discloses all the elements of the claimed invention as mentioned in claim 7 above but fails to explicitly disclose that the specified code is zero.

Chan discloses an IC tag (via RF tag 120, see fig. 3) wherein the transponder transmits the data when the counter (via state counter 432) of the tag is at predetermined value, which is zero (see col. 6, lines 19-23).

From the teaching of Chan it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the IC tag of Bandy to have the tag transmit its data when the specified value of the counter is zero in order to make the interrogation process simpler and reduce the chances of collision.

9. Claims 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bandy (6,002,344) and Raimbault (6,177,858) as applied to claim 10 above, and further in view of Chan (5,550,547).

The combination of Bandy and Raimbault discloses all the elements of the claimed invention as mentioned in claim 10 above, but fails to explicitly disclose that the specified code is zero.

Chan discloses an IC tag (via RF tag 120, see fig. 3) wherein the transponder transmits the data when the counter (via state counter 432) of the tag is at predetermined value, which is zero (see col. 6, lines 19-23).

Response to Arguments

10. Applicant's arguments filed 5/28/08 have been fully considered but they are not persuasive. Applicant argues that counter/shiftregister of Bandy is "not a memory address counter that stores a bit address of the memory pertaining to the first information". The Examiner respectfully disagrees. Applicants are reminded that during examination, claims are given their "broadest reasonable interpretation" *In re Morris*, 127 F.3d 1048, 1054, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997); *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969).¹ Therefore, under the broadest reasonable interpretation standard, the Examiner maintains her interpretations.

In Remarks (filed 5/23/08, page 10, lines 11-22), applicant discloses that the structure of the memory address counter in the present application and the counter/shift

¹ 19 See also MPEP §2111; *In re Graves*, 69 F.3d 1147, 1152, 36 USPQ2d 1697, 1701

register of Bandy is totally different. From the specification (paragraph [0034] of published application), "the memory address counter 13 is a counter indicating bit address of the memory 16 and has the same bit number as the first random number 11." Specification does not disclose that memory address counter indicates the bit address of the first information or the second information since both the first and second information is contained in the memory 16. Since the tag 102 of Bandy transmits the response signal when the value of the counter is equal to tag ID (tag IDs are stored in the memory), it is indicating the bit address of memory, namely the tag ID number, the manufacture number and the lot number. Bandy further discloses that counter/clock 406 of the reader has the same number of counts as counter 32 of tag, and when a tag sends a response signal it does not have to transmit the tag ID, just a simple response signal without any information would be enough for the reader to know the tag ID because the counts in the counter 406 of the reader are the same as counts in the counter 312 of tag. This definition shows that counter is indicating the memory address by indicating the tag ID number (see col. 7, lines 1-33).

From the discussion given above, Examiner interprets that the memory address counter indicates the bit address of the memory and this limitation is taught by Bandy as explained above, hence Examiner maintains his interpretation of the claim.

Conclusion

Art Unit: 2612

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to NABIL H. SYED whose telephone number is (571)270-3028. The examiner can normally be reached on M-F 7:30-5:00 alt Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Zimmerman can be reached on (571)272-3059. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nabil H Syed
Examiner
Art Unit 2612

N.S

/Brian A Zimmerman/
Supervisory Patent Examiner, Art Unit 2612